SENSE AMPLIFIERS WITH OUTPUT BUFFERS AND MEMORY DEVICES INCORPORATING SAME

ABSTRACT OF THE DISCLOSURE

A memory device includes a memory cell array including a plurality of memory cells and cell select circuitry configured to selectively connect the plurality of memory cells to a data line, e.g., a common output node of a column selecting gate circuit. The device further includes a bias circuit operative to charge the data line to a bias voltage responsive to a bias enable signal, and a sense amplifier circuit having an input coupled to the data line and including an output buffer. The sense amplifier circuit is operative to drive the output buffer according to a voltage on the data line responsive to a sense enable signal to thereby generate a sense amplifier output signal indicative of a state of a memory cell connected to the data line.